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vyh@nt-rt.ru || https://vishay.nt-rt.ru/

5 V, 1 A H-Bridge Motor Driver

DESCRIPTION

The SIP2100 is an integrated, buffered H-bridge with TTL and CMOS compatible inputs with the capability of delivering up to 1 A continuous current at 5 V V_{DD} supply.

The SIP2100 has two independent logic inputs that can set four different motor operation modes: normal rotation, reverse rotation, stop (idling) and braking. The internal shoot-through protection logic also prevents upper and lower outputs from being turned on simultaneously.

The SiP2100 offers high efficiency with an extremely low operating current. The device also benefits from over temperature protection with a shut down hysteresis of 20 °C.

The SIP2100 is available in SOIC8 package.

FEATURES

- 1 A drive capability
- Optimized for 5 V V_{DD} bias
- Extremely low idle current
- Shoot-through protection scheme
- Thermal shutdown

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- High performance servo
- Optical/tape disk drives
- Brush/stepper motor driver

PACKAGE OUTLINE

SOIC (Top View)

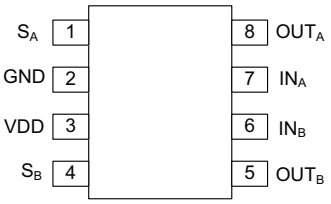


Fig. 1 - Package and Pinout

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE

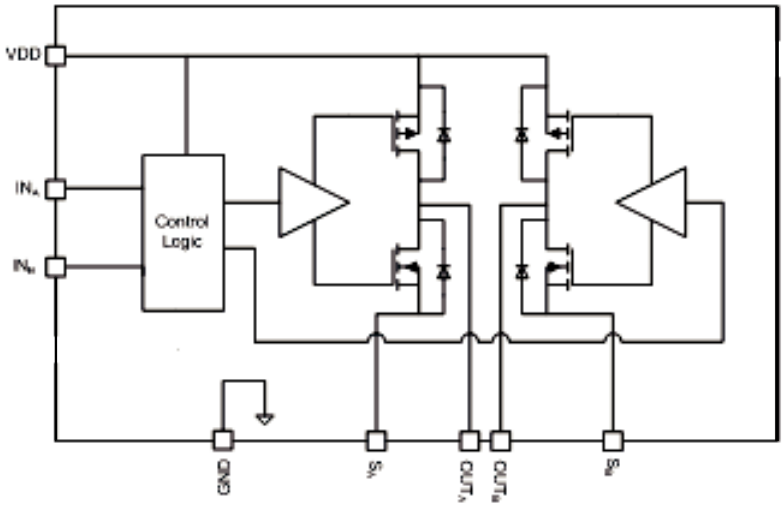


Fig. 2 - Functional Block Diagram

TRUTH TABLE

IN_A	IN_B	OUT_A	Out_B
1	0	1	0
0	1	0	1
0	0	0	0
1	1	HiZ	HiZ

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Electrical Parameter	**Conditions**	**Limits**	**Unit**
V_{DD}	Reference to GND	- 0.3 to 6	V
OUT_A, OUT_B	Reference to GND	- 0.3 to 6	
S_A, S_B	Reference to GND	- 0.3 to 1	
IN_A, IN_B	Reference to GND	- 0.3 to V_{DD}	
Temperature			
Operating Temperature		- 40 to 85	°C
Max. Operating Junction Temperature		150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS				
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	3.8	5	5.5	V
Temperature				
Operating Junction Temperature	0		125	°C
Recommended Ambient Temperature	0		70	

THERMAL RESISTANCE RATINGS			
Parameter		**Max.**	**Unit**
Thermal Resistance (Junction to Ambient)	SO-8, R_{thJA}	153	°C/W
	SO-8 PowerPAD, R_{thJC}	40	
Power Dissipation	SO-8, T_A = 70 °C	522	mW
	SO-8 PowerPAD, T_A = 70 °C	2	W
Junction Temperature		- 65 to 150	°C
Storage Temperature		- 55 to 150	

SPECIFICATIONS (T_A = 25 °C, unless otherwise specified)							
Parameter	**Symbol**	**Test Conditions V_{DD} = 5 V**		**Limits**			**Unit**
				Min.[a]	**Typ.[b]**	**Max.[a]**	
Driver Power Supply							
V_{DD} Bias Supply Current	I_{DD}	IN = 100 kHz			250	300	µA
		IN = 20 kHz			150	180	
		Quiescent state			50		
V_{DD} Rising Threshold	$V_{DD\ TH\_R}$	V_{DD} rising			2.8	3	V
V_{DD} Falling Threshold	$V_{DD\ TH\_F}$	V_{DD} falling		2	2.5		
V_{DD} UVLO Hysteresis	$V_{DD\ UVLO}$				300		mV
Input Logic							
Input Voltage High	VIN_H			2			V
Input Voltage Low	VIN_L					0.7	
Input Sourcing Current	I_{INH}					1	µA
Input Sinking Current	I_{INL}			- 1			
Output Stage							
Output Voltage High	V_{OUTH}	I_{OUT} = - 500 mA	V_{DD} = 4.75 V	4.4			V
		I_{OUT} = - 1000 mA		4.25			
Output Voltage Low	V_{OUTL}	I_{OUT} = + 500 mA				0.25	
		I_{OUT} = + 1000 mA				0.5	
Output High Propagation Delay	TP_{LH}				20	25	nS
Output Low Propagation Delay	TP_{HL}				20	25	
Thermal Protection							
Thermal Shutdown Threshold					150		°C
Thermal Shutdown Hysteresis					20		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

PIN DESCRIPTION (SOIC PACKAGE)		
Pin Number	**Name**	**Function**
1	S_A	Driver output return A
2	GND	Analog ground of internal logic
3	V_{DD}	Input of internal logic bias and power stage
4	S_B	Driver output return B
5	OUT_B	Driver output B
6	IN_B	Driver input B
7	IN_A	Driver input A
8	OUT_A	Driver output A

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

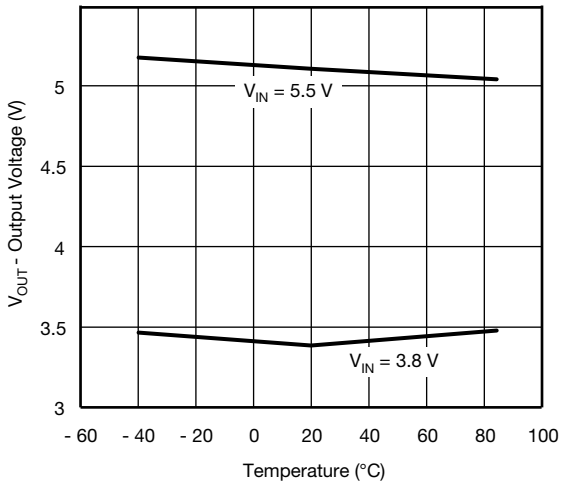


Fig 1. Output Voltage vs. Temperature (at 1.5 A Load)

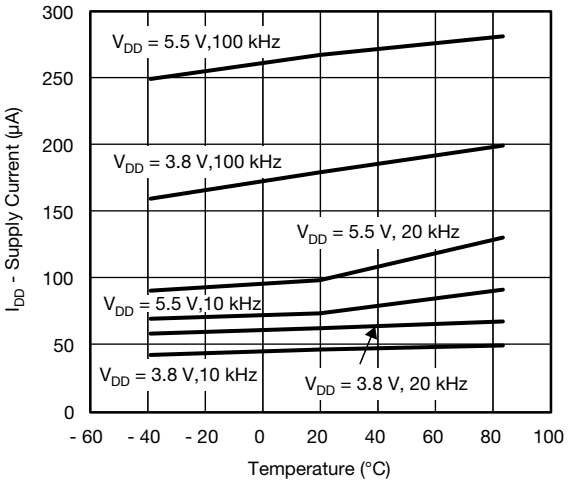


Fig 2. Supply Current I_{DD} vs. Temperature

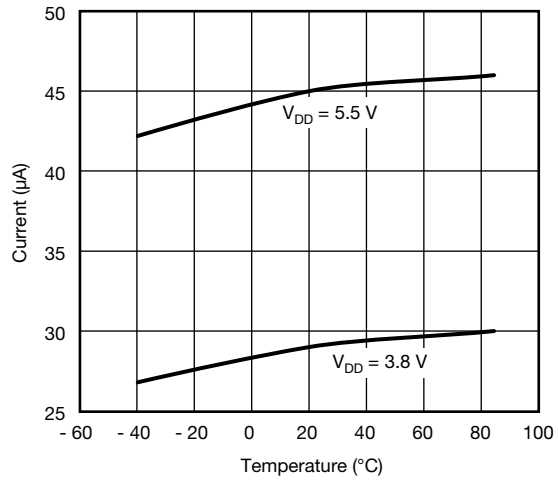


Fig 3. Quiescent Current vs. Temperature

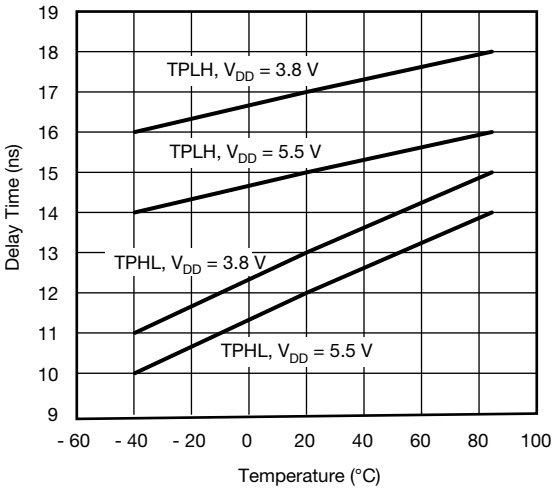


Fig 4. Propagation Delay vs. Temperature

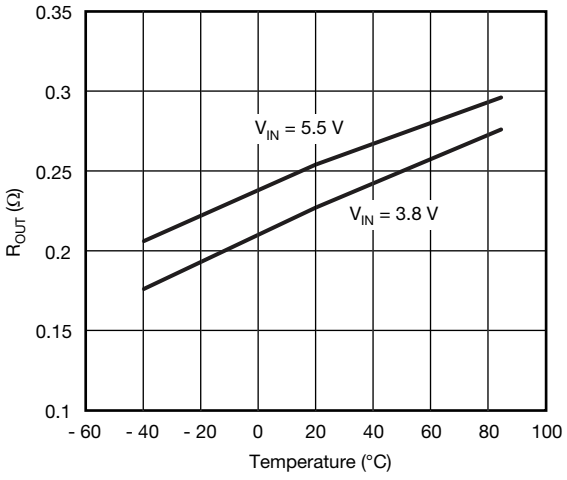


Fig 5. R_{OUT} vs. Temperature

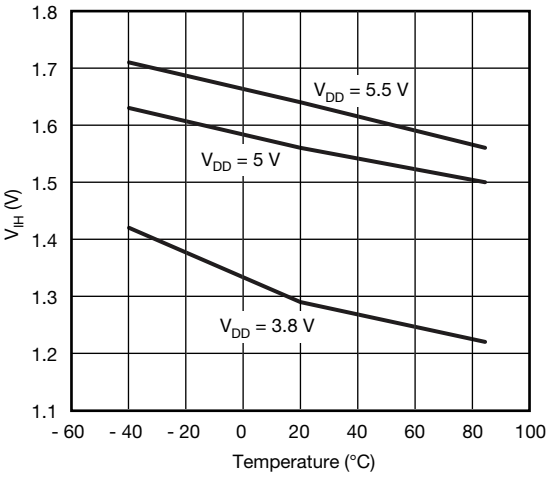


Fig 6. PWM Rising Threshold vs. Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

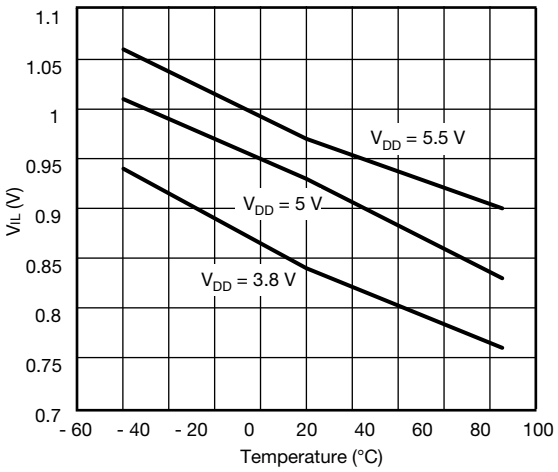
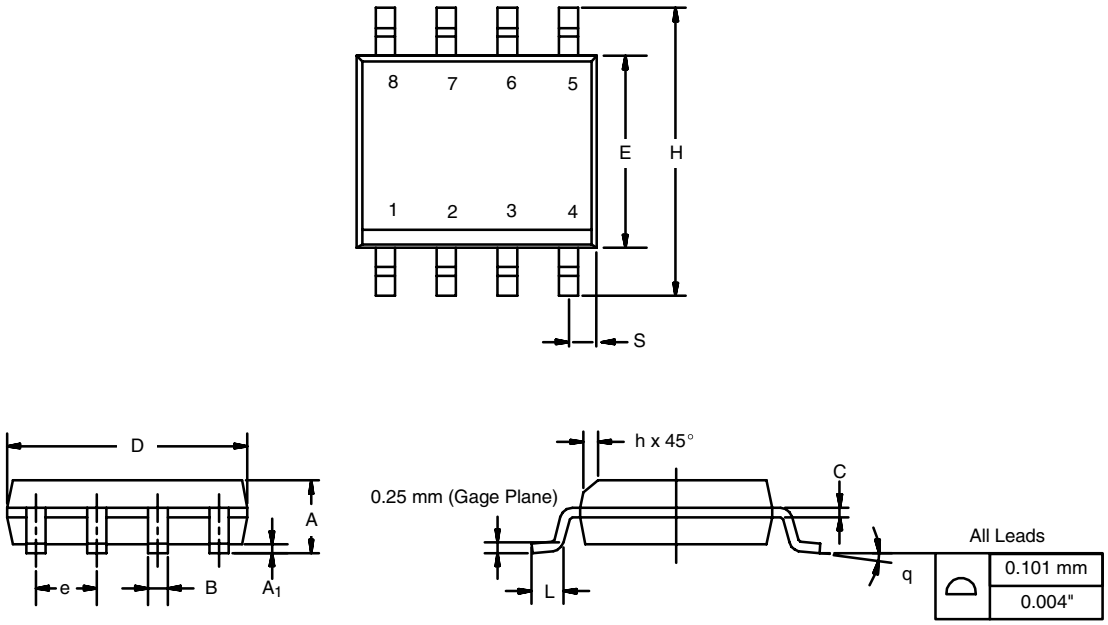


Fig 7. PWM Falling Threshold vs. Temperature

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

Battery Monitor and Protective Discharge IC

DESCRIPTION

The SiP31001 protects a single cell Li-Ion battery from over voltage under elevated temperature condition.

Elevated temperature and allowing the battery to sit at the maximum charge voltage for extended periods of time will cause shorter than expected battery life. SiP31001 enables the battery to relax after charged even when kept on float or trickle charge.

The SiP31001 discharges battery at constant 100 mA when pre-set safe guard limits of both battery voltage and temperature are exceeded. The discharge will stop once either the battery voltage or temperature falls below the thresholds.

The SiP31001 wakes up to monitoring mode when battery voltage is over 4 V. Under this state, the monitoring circuit is on every 2 s for a 5 ms duration, conducts precise comparison of voltage and temperature to pre-set limits. Such design scheme minimizes the power consumption.

The SiP31001 integrates an over temperature protection that will switch off the constant current discharge switch when the device is over heated.

TST pin enables the production test of discharge switch without forcing excessive voltage.

The SIP31001 is available in compact WCSP9 of 1.25 mm x 1.25 mm.

FEATURES

- Wide operation voltage range: 2.3 V to 5.5 V
- Low quiescent current: 330 nA
- Constant current discharge: 100 mA
- Precision battery voltage and temperature monitoring circuit thresholds
- ESD
  - Human body model: 4 kV
  - Machine model: 400 V
  - Air discharge: 15 kV
  - Contact discharge: 8 kV
- Ultra compact WCSP9, 1.25 mm x 1.25 mm

APPLICATIONS

- Cellular phones, smart phone
- Tablet devices
- Portable media players
- Digital cameras
- One cell Li-Ion battery power devices

TYPICAL APPLICATION CIRCUIT

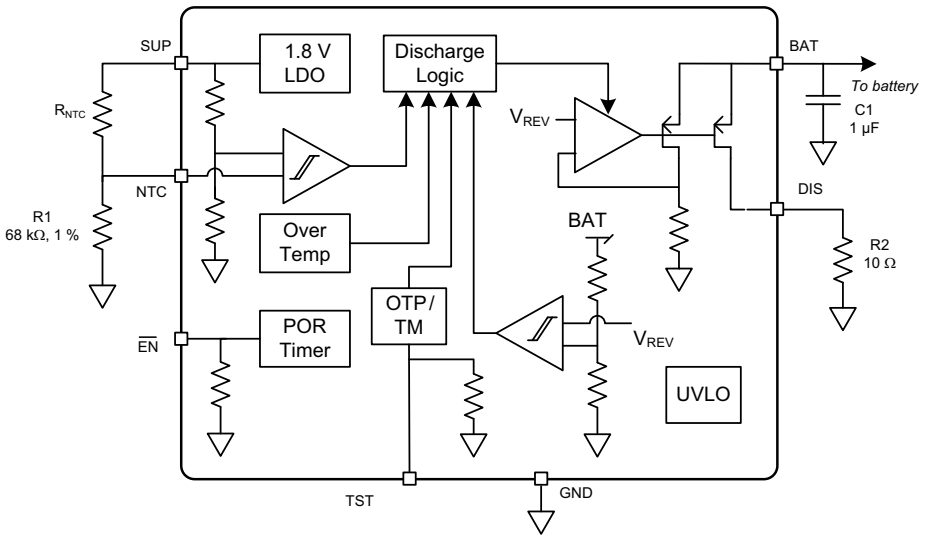
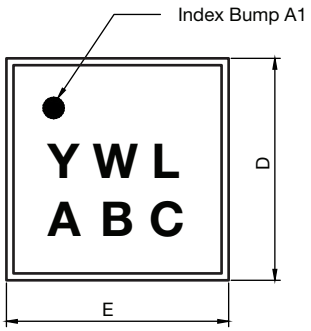


Fig. 1 - Typical Application Circuit

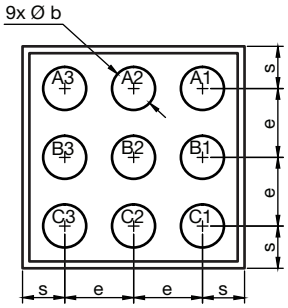
Note

- Above design example targets 60 °C over temperature trigger and 55 °C over temperature release. R1 is 68 kΩ 1%, and R_{NTC} is Murata, NCP03WF104F05RL

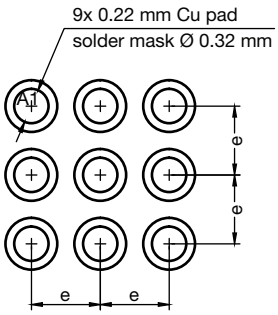
WLCSP9 3 x 3 (9 Bumps) POD (for 17 mil Die thickness)



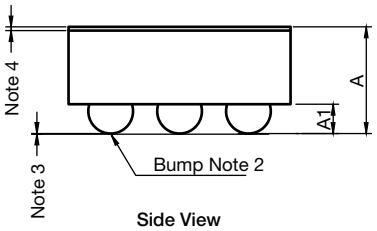
Top View



Bottom View



Recommanded
Land Pattern
(NSMD)



Side View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.600	0.620	0.640	0.0236	0.0244	0.0252
A1	0.144	0.170	0.196	0.0057	0.0067	0.0077
b	0.220	0.250	0.280	0.0087	0.0098	0.0110
e		0.400			0.0157	
s	0.205	0.225	0.245	0.0081	0.0089	0.0096
D	1.220	1.250	1.280	0.0480	0.0492	0.0504
E	1.220	1.250	1.280	0.0480	0.0492	0.0504

Notes (unless otherwise specified)

1. Laser mark on the silicon die back, coated with an epoxy film.
2. Bumps are SAC396.
3. 0.050 mm max. co-planarity.
4. Laminate tape thickness is 0.022 mm.
5. Use millimeters as the primary measurement

T14-0805-Rev. A, 29-Dec-14
DWG: 6030

Precision Threshold Logic Gate Switch

DESCRIPTION

The SiP32205 is an integrated logic AND switch with a precision logic threshold. The output is driven high only when both inputs are high, otherwise it is held low. The device features low quiescent current and fast switching capability.

The two logic inputs have extremely low input capacitance and a tightly controlled threshold voltage between 1 V to 1.3 V over the operating range.

The logic inputs also have integrated 100 kΩ pull down resistors.

To prevent glitches during power up, internal circuitry will hold the output low until the supply voltage has settled.

The SiP32205 is available in (Pb)-free, 6 bump, 0.8 mm x 1.2 mm WCSP package, with 0.4 mm pitch. The package has black polyethylene top side lamination to reduce light sensitivity and improve ruggedness.

FEATURES

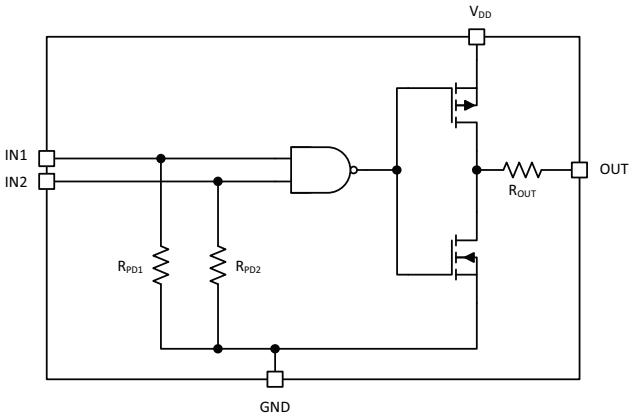
- Wide input voltage, 2 V to 5 V
- Two logic inputs with integrated 100 kΩ pull down resistors
- < 10 pF logic input capacitance
- < 1 kΩ output pull-up/pull-down resistors
- Compact 6-bump WCSP package with top side lamination

Pb-free
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

APPLICATIONS

- Portable devices
- Peripherals and accessories

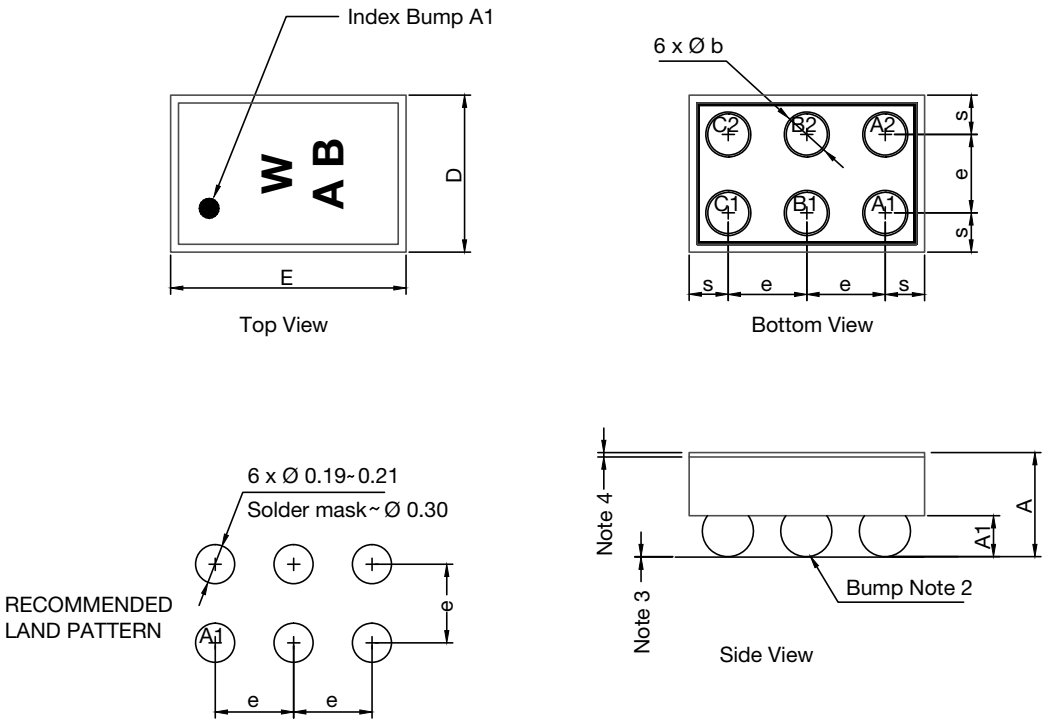
EQUIVALENT CIRCUIT



TRUTH TABLE		
IN1	**IN2**	**V_{DD} to OUT**
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

WCSP6: 6 Bumps

(2 x 3, 0.4 mm pitch, 208 µm bump height, 0.8 mm x 1.2 mm die size)



DIMENSION	MILLIMETERS [5]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.515	0.530	0.545	0.0203	0.0209	0.0215
A1	0.183	0.208	0.233	0.0072	0.0082	0.0092
b	0.234	0.260	0.312	0.0092	0.0102	0.0123
e		0.400			0.0157	
s	0.160	0.180	0.200	0.0063	0.0071	0.0078
D	0.720	0.760	0.800	0.0283	0.0299	0.0315
E	1.120	1.160	1.200	0.0441	0.0457	0.0472

Notes (unless otherwise specified)

(1) Laser mark on the silicon die back coated with an epoxy film.
(2) Bumps are SAC396.
(3) 0.050 max. co-planarity.
(4) Laminate tape thickness is 0.022 mm.
(5) Use millimeters as the primary measurement.

ECN: S13-1793-Rev. A, 26-Aug-13
DWG: 6018

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