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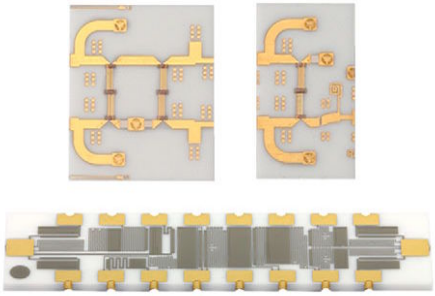
Custom Substrates - Metal Via / Multilayer / Lumped Element



FEATURES

- Plated or filled via technology
- Mulitlayer and overcoat patterning
- Lumped element custom substrates
- Al_2O_3, AlN, and BeO substrate drilling and shaping
- TaN and NiCr resistor films
- Metallization on 1,2, or 4 surfaces
- Various substrate materials
- Sputtered / plated metal systems
- Custom sizes from 0.020" x 0.020" to 4.000" x 4.000"
- Quick delivery available

APPLICATIONS

Vishay EFI custom interconnect substrates are used in military, aerospace, hybrid circuit, telecommunications, microwave, and industrial applications. These custom interconnect substrates are manufactured to be used in heat transfer connectors, top to bottom connectors, and RF / microwave designs. Surface connections can be made by plated thru-holes, edge wraps, or filled via technologies. Custom cutouts of various sizes and shapes can also be created and used to fit into almost any size and shape. The custom interconnect substrates are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The custom interconnect substrates are 100 % electrically tested (when applicable) and visually nspected to MIL-STD-883, method 2032 class H or K.

FRONT TO BACK CONTINUITY

For designs requiring metal or electrical connection from the top to the bottom of the substrate, metal via connections will be used. Metalized Edge Wraps are chosen for applications where soldering to the side of the substrate is desired for connection to the PCB or module design. Plated thru-holes are used for applications where the module design may require alignment or soldering pins to be inserted into the holes. Filled vias are used for applications where the strongest electrical connection is needed or preventing solder migration to the backside. See Fig. 1 below for edge wrap, plated thru-hole, and filled via pictorial representation.

METALLIZED EDGE WRAPS	
Min. distance from wrap edge to pattern edge	0.005"
Min. tolerance from wrap center to pattern edge	± 0.002"
Wrap diameter (as measured from exit side)	0.8 to 2.0 x substrate thickness

PLATED THRU-HOLES	
Min. distance from hole edge to pattern edge	0.005"
Min. tolerance from hole center to pattern edge	± 0.002"
Hole diameter (as measured from exit side)	0.8 to 2.0 x substrate thickness
Min. hole center to hole center spacing	2 x hole diameter

FILLED VIAS	
Min. distance from via edge to pattern edge	0.0025"
Min. tolerance from via center to pattern edge	± 0.002"
Min. via center to via center spacing	2 x via diameter
Preferred via diameter (as measured from exit side)	0.8 x substrate thickness
Via diameter range (as measured from exit side)	0.6 - 1.5 x substrate thickness
Min. via diameter	0.007"
Max. via diameter	0.040"

Note

- These rules apply to the non-vented via side

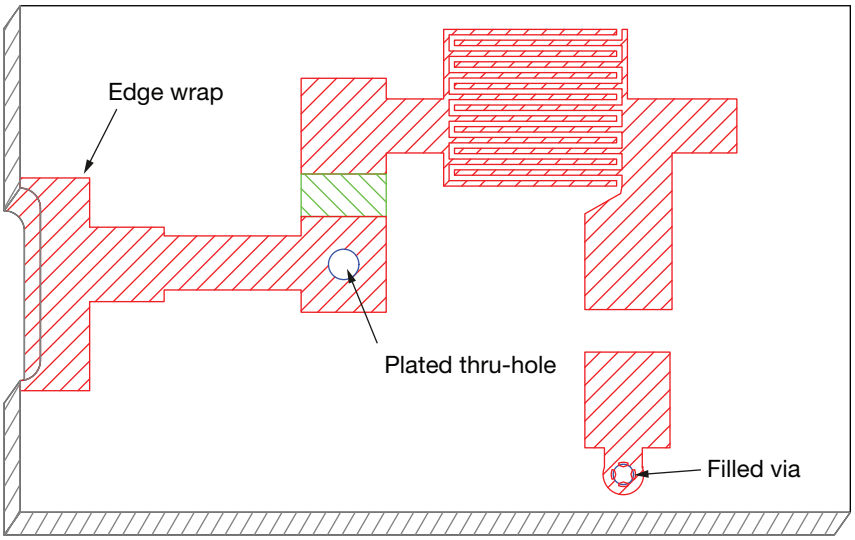


Fig. 1

FILLED VIA VENT NOTES	
Min. distance from via vent edge to pattern edge	0.004"

Note

- Via vents are required on one side of the substrate if metals are plated
- See Fig. 2 for via vent pattern example

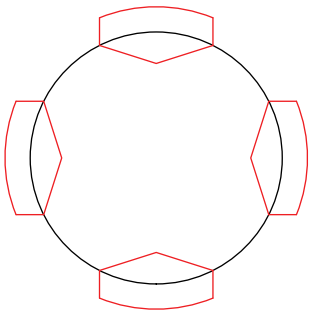


Fig. 2

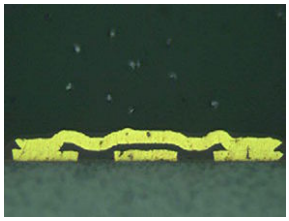
SHAPES AND CUT-OUTS

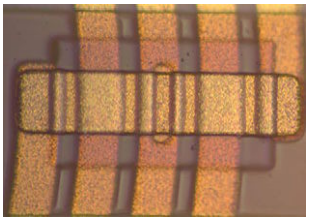
Many circuit designs require custom substrates with different shapes and holes cutout of the parts. These include cutting out material internal and external to the overall part size and shape.

PART SHAPE / CUT-OUTS	
Min. distance from cut-out edge to pattern edge	0.003"
Min. tolerance from cut-out edge to pattern edge	± 0.002"
Min. tolerance of cut-out feature	± 0.003"
Min. distance between cut-outs	0.050"

MULTILAYER AND AIR BRIDGE

For certain complex designs multiple layers of metal and / or interlevel dielectrics are required. Vishay Electro-Films has developed precision patterning and layering techniques where ± 0.0001" pattern tolerance and ± 0.0005" layer to layer alignment is achievable.





For Multilayer designs that require an interlevel dielectric the following two choice are currently available:

DIELECTRIC	TYPICAL THICKNESS	PATTERN TOLERANCE	DIELECTRIC CONSTANT
Silicon nitride (1)	4000 Å to 6000 Å	± 0.002"	-
Polyimide	50 000 Å to 80 000 Å	± 0.002"	3.2 at 1 MHz

Note

(1) Silicon nitride can also be used to integrate a capacitive element to the design if needed

In applications where lange couplers and cross-metal patterning are needed, air bridges can be used to connect different metal patterns using polyimide supported bridges. These bridges require several design guidelines for layering the base metal, polyimide, and bridge metal into the optimum air bridge design.

Fig. 3 can be used as a guideline for a typical lange coupler / air bridge set-up. The dimensions listed in the bubble detail picture are considered minimums for any design. For more specific design layout guidelines, contact the factory for more information.

MULTI-LEVEL CROSSOVER DESIGN PARAMETERS			
PARAMETER		MINIMUM VALUE (in µm)	COMMENTS
Dimension	Crossover thickness	0.0001 (2.5)	Minimum
A	Crossover width	0.001 (25)	0.0001 in crossover to conductor pullback
B	Crossover length	0.003 (75)	Minimum
C / D	Insulator dimension	Length: 0.0015 (37.5) Width: 0.003 (76)	0.0025 (63) insulator-to-conductor overlap
	Insulator material		Polyimide
E / F	Encapsulation dimension	Crossover width: +0.0015 (37.5) Crossover length: +0.003 (76)	These values are added to the insulator dimension
	Encapsulation material		Polyimide

Note

- These rules apply to the non-vented via side

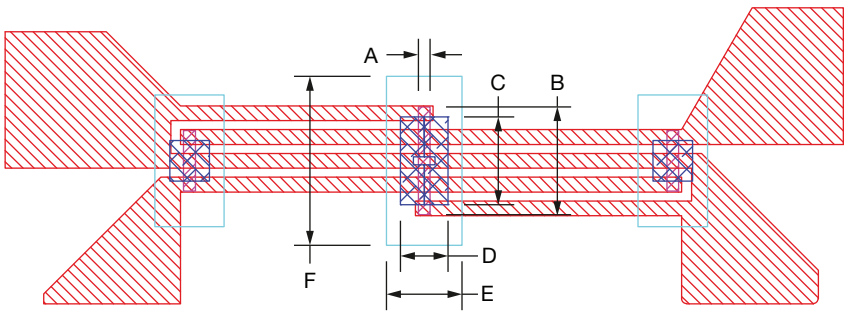
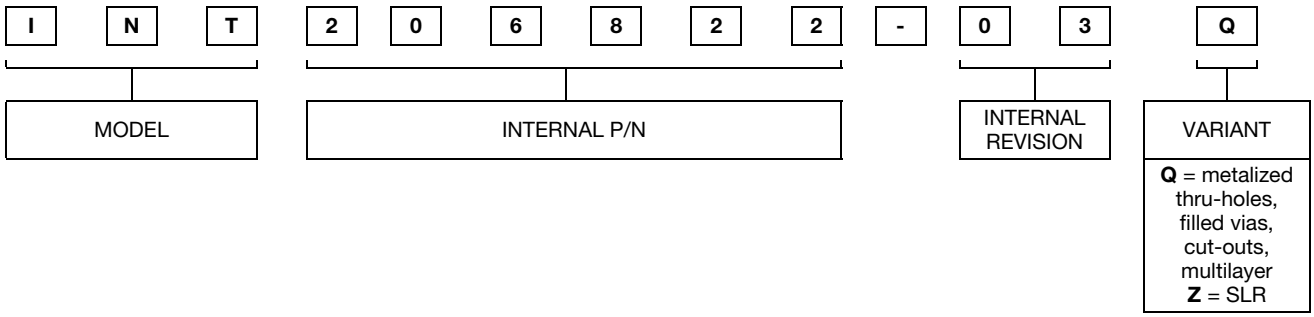


Fig. 3

GLOBAL PART NUMBER INFORMATION

Custom Global Part Number: INT206822-03Q

Custom Global Part Number Description: interconnect custom 206822-03Q



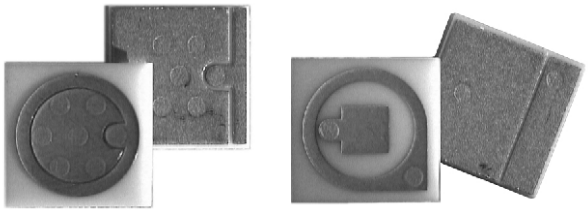
Note

- Z = SLR,

LSUB

Vishay Electro-Films

Ceramic Submount for High Power LED



The LSUB series substrates are ceramic LED package bases designed to provide thermal management for high power (> 1 W) LED devices; the LSUB is designed to minimize the thermal resistance between the die junction and the package termination. The LSUB's enhanced thermal management enables a lower junction temperature and increased efficiency and reliability compared to other technologies. In addition to the increased brightness, the lower junction temperature results in better color uniformity.

The LSUB is available in two configurations; in the standard configuration the LED die is mounted directly over filled vias and an offset version where the filled via is located to the side of the die pad. The standard configuration is designed for the attach methods including conductive epoxies and thick solders (greater than 12 µm) while the offset configuration is designed for thin eutectic solder layers in the 2 µm to 3 µm range. An additional benefit of the standard configuration is the pad size is large enough to accommodate a parallel diode for ESD protection.

The LSUB is available singulated as individual die or in square arrays. Additional LED configurations and form factors available upon reques.

FEATURES

- Ultra-low thermal resistance
- Eutectic or epoxy LED die attach pads
- Surface-mounted component assembly

APPLICATIONS

- High power LED for automotive, industrial and home applications
- High power laser diodes for industrial applications

GENERAL SPECIFICATIONS	
Substrate Material	Alumina 99.6 %, Alumina 96 % or AlN
Conductor Material	Copper
Conductor Thickness	5 µm ± 10 %
Substrate Thickness	25 mil (0.635 mm)
LED Die Size	40 mil x 40 mil (1 mm x 1 mm)
Operating Temperature (°C)	- 55 to + 125
Storage Temperature (°C)	- 55 to + 125
Die Bond Pad Metallization	Ni/Au or 80 %/20 % AuSn over Ni/Au

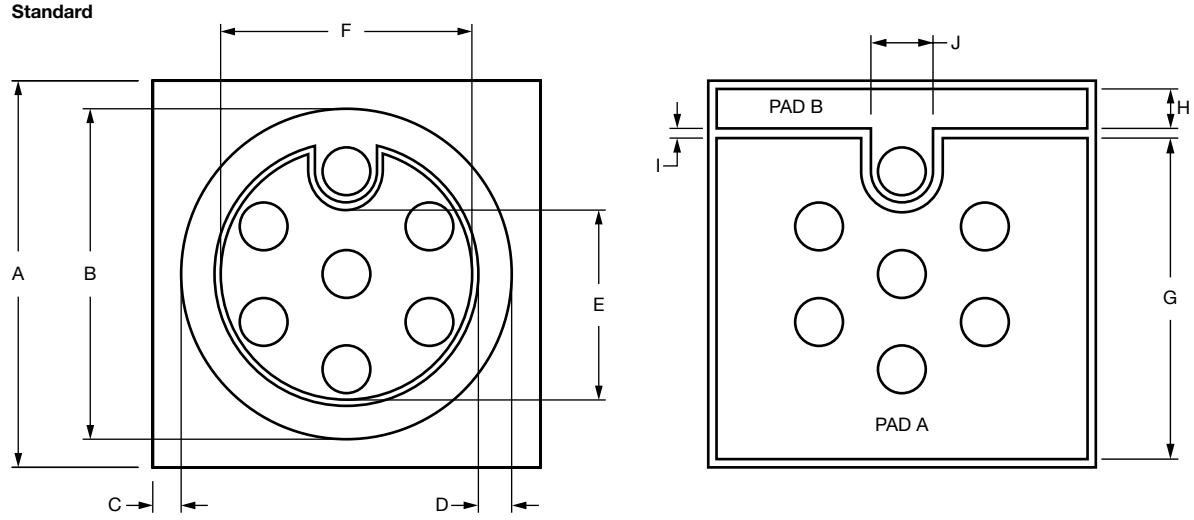
TYPICAL THERMAL RESISTANCE (1) (K/W)		
SUBSTRATE	**STANDARD**	**OFFSET**
AlN	3	5
Alumina (99.6 %)	6	8
Alumina (96 %)	10	12

Note

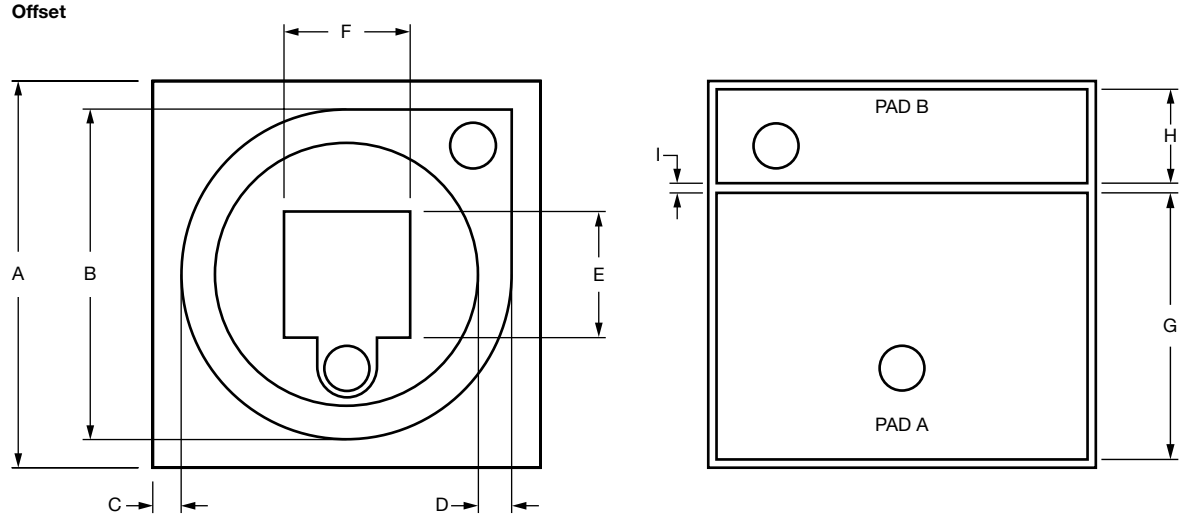
(1) Thermal resistance between die pad and package termination (anode)

DIMENSIONS

Standard



Offset



DIMENSIONS in inches (millimeters)		
DIMENSION	**STANDARD**	**OFFSET**
A	0.138 (3.500)	0.138 (3.500)
B	0.118 (3.000)	0.118 (3.000)
C	0.010 (0.254)	0.010 (0.254)
D	0.012 (0.300)	0.012 (0.300)
E	0.068 (1.727)	0.045 (1.143)
F	0.090 (2.286)	0.045 (1.143)
G	0.114 (2.896)	0.095 (2.413)
H	0.014 (0.356)	0.033 (0.838)
I	0.003 (0.076)	0.003 (0.076)
J	0.016 (0.406)	n/a

GLOBAL PART NUMBER INFORMATION

Global Part Number: LSUBNSPL

Global Part Number Description: LSUB, AIN, standard, plate

L	S	U	B	N	S	P	L

MODEL	Substrate	Surface	PACKAGING CODE
LSUB	**N** = AlN **A** = Alumina 99.6 % **T** = Alumina 96 %	**S** = Standard **O** = Offset	**PL** = Plate **SC** = Scribed plate **ST** = Diced on tape **WS** = Waffle pack

LAYOUT CONSIDERATIONS

The thermal performance of the LSUB package is strongly influenced by PCB layout. The package ensures that heat flows from the die junction to the package termination (anode); however, the heat must be carried from the termination by the PCB layout. Special consideration must be given to insure minimal thermal resistance between the package termination and the ambient. The following guidelines should be considered.

- The filled vias in the standard configuration can be up to 0.5 mils lower than the surrounding surface, when mounting dies on top of these vias care should be taken to use an attachment method capable of overcoming this surface profile.
- The traces that carry current to and from the component also carry the heat away from the component. These traces should be made as wide and thick as possible to help spread the heat on the PCB.
- The LED die should be kept as far as possible from other hot components such as DC circuitry, FETs and inductors.
- Heat sink elements are to be positioned as closely as possible to the LED package.

Custom Substrates - Conductor Resistor Pattern and Overcoat

FEATURES

- Precision conductor and resistor patterns
- TaN and NiCr resistor films
- Resistor tolerance down to 0.1 %
- Silicon nitirde, and polyimide overcoat coatings
- Metallization on 1 or 2 surfaces
- Various substrate materials
- Sputtered / plated metal systems
- Custom sizes from 0.020" x 0.020" to 4.000" x 4.000"
- Quick delivery available

APPLICATIONS

Vishay EFI conductor resistor patterned substrates with optional overcoat coatings are used in the hybrid circuit, microwave, and telecommunications industries. These conductor resistor patterns are precisely manufactured to be used for precision current flow, voltage division and RF / Microwave designs. Resistor overcoat options are used for resistor protection and can be applied and patterned to match the conductor and / or resistor pattern. The conductor resistor patterned substrates are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The custom specialty film substrates are visually inspected to MIL-STD-883, method 2032 class H or K.

INTEGRATING THIN FILM RESISTORS

Vishay EFI offers two thin film resistor film choices of lithographically patterned Tantalum Nitride (TaN) or Nickel Chromium (NiCr). The resistive film should be selected based upon application-specific requirements such as performance, assembly packaging needs, and temperature exposure. The table below summarizes the key standard parameters of these resistor materials.

STANDARD THIN FILM RESISTOR PARAMETERS

MATERIAL	TCR (ppm/°C)	STANDARD SHEET RESISTIVITY 99.6 % Al_2O_3 (Ω/sq)	STANDARD SHEET RESISTIVITY AIN, BeO (Ω/sq)	STABILITY (1)	TOLERANCE (2)
TaN	± 50	20 to 125	25 to 100	< 0.1 %	0.1 % to 20 %
NiCr	± 25	25 to 225	50 to 150	< 0.1 %	0.1 % to 20 %

Notes

(1) 1000 h at 125 °C in air

(2) Special tolerances available

CURRENT DENSITY

To ensure optimal Resistor performance, the design engineer must consider the self-heating effects of the operating resistor and understand the power dissipation characteristics of the environment. A complete thermal analysis should be performed by the design engineer to ensure proper thin film resistor design. The following table lists current density standards for common materials.

CURRENT DENSITY					
SHEET RESISTANCE	Al_2O_3	SILICON	QUARTZ	AIN	BeO
25 Ω/sq	4 mA/mil	20 mA/mil	0.5 mA/mil	19 mA/mil	32 mA/mil
50 Ω/sq	2 mA/mil	10 mA/mil	0.25 mA/mil	9.5 mA/mil	16 mA/mil
100 Ω/sq	1 mA/mil	5 mA/mil	0.125 mA/mil	4.7 mA/mil	8 mA/mil
200 Ω/sq	0.5 mA/mil	2.5 mA/mil	0.062 mA/mil	2.3 mA/mil	4 mA/mil

RESISTOR DESIGN

After the thin film resistor values have been determined and a metallization film selected per SPF1 and SPF2 datasheets, the thin film resistor layout can be designed. There are two typical approaches for accomplishing this: the block-style resistor (see Fig. 1) or serpentine- style resistor (see Fig. 2). With both design approaches, it is standard to employ a laser trim process to trim the resistor to the desired value and tolerance. Vishay EFI employs both scrub (edge) trimming and plunge trimming techniques to achieve the desired resistor value.

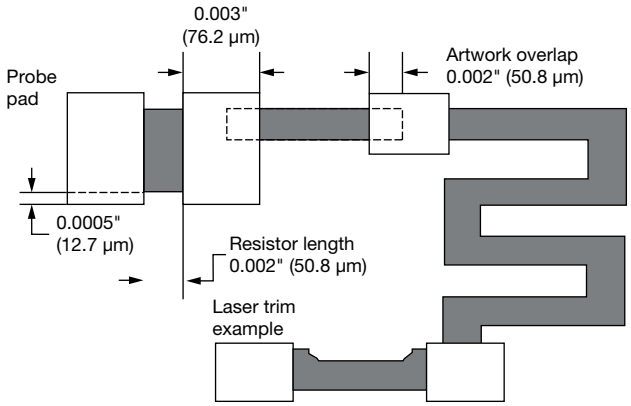


Fig. 1 - Probe pad and artwork overlap requirements (minimum)

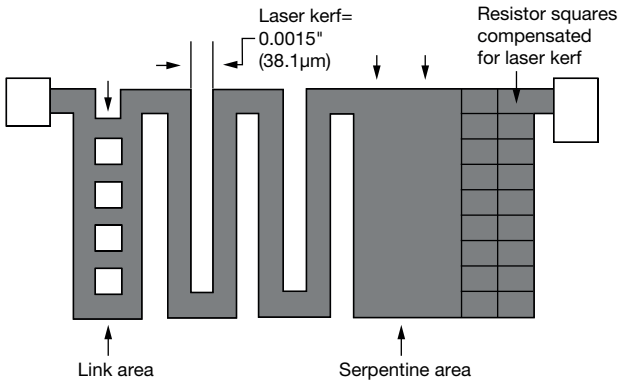


Fig. 2 - Serpentine resistor with two areas for laser trim

RESISTOR DESIGN RULES		
PARAMETER	VALUES	COMMENTS
Min. resistor dimension	0.002" x 0.002" (50 µm x 50 µm)	
Min. probe pad dimension	0.003" x 0.003" (75 µm x 127 µm)	For resistors < 1000 Ω, use probe pad size of 0.006" (152 µm) x 0.008" (203 µm)
Min. conductor/resistor design overlap	0.002" (50 µm)	See Fig. 1
Resistor layout dimensions (block resistor/serpentine resistor)	100 % of nominal value / 100 % of nominal resistor value plus laser kerfs of 0.5 mil^2/sq	
Resistor trim	Scrub, plunge, or bake to value	Bake to value ± 10 % or 20 %

All high frequency resistors should be Edge trimmed to value to preserve frequency response. VEFI can also supply resistors of 20 % tolerance (10 % special) or looser tolerances which are designed to 100 % of bake to value with no laser trimming.

PROTECTIVE COATING

Vishay Electro-Films (EFI) has developed several patternable overcoat options to protect the resistors and other critical areas from mechanical damage during handling. It is essential to overcoat resistors of 0.1 % or tighter tolerances to maintain tolerance during assembly and test of the hybrid, and it is beneficial to overcoat all resistors.

PROTECTIVE COATING APPLICATIONS

OVERCOAT	TYPICAL THICKNESS (Å)	APPLICATIONS
Silicone nitride	4000 to 6000	Resistor overcoat with fine trim capability and integrated capacitor
Polyimide	50 000 to 80 000	Resistor overcoat and solder dam

PROTECTIVE COATING GUIDELINES

OVERCOAT	TYPICAL THICKNESS (Å)	MIN. FEATURE SIZE	MIN. METAL OVERLAP	PATTERN TOLERANCE (1)
Silicone nitride	4000 to 6000	0.004" x 0.004"	0.002"	± 0.002"
Polyimide	50 000 to 80 000	0.004" x 0.004" (2)	0.001"	± 0.002"

Notes

(1) Special tolerance of ± 0.001" available

(2) Minimum gap in polyimide pattern is 0.0015" x 0.003"

In summary NiCr will perform at higher sheet resistance with lower TCR than TaN giving higher resistance values in less area. TaN will continue to perform in a moisture environment but NiCr will require a hermetic package to maintain resistance values. Both resistive films will work in highly demanding environments for a wide range of applications with VEFI thin film technology.

GLOBAL PART NUMBER INFORMATION

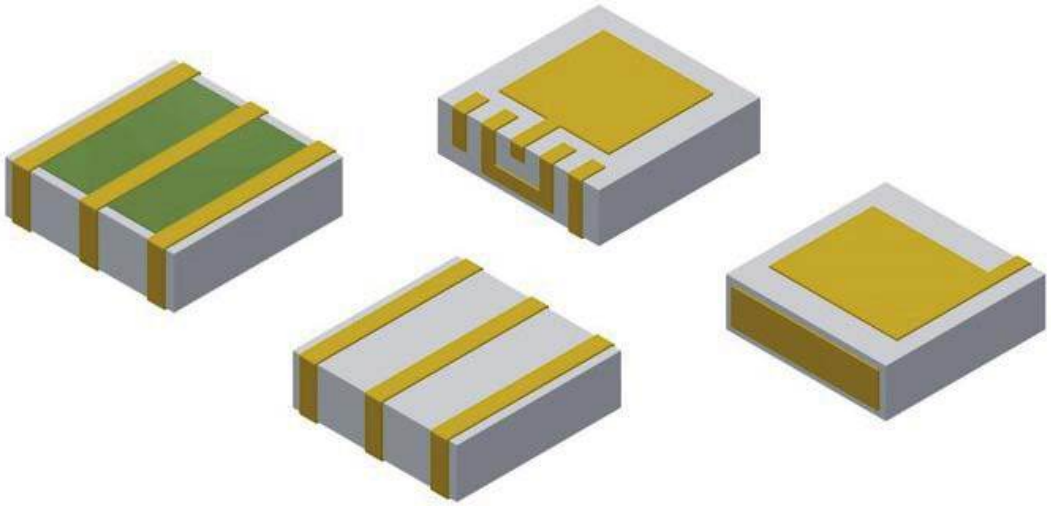
Custom Global Part Number: PSS205687-00N

Custom Global Part Number Description: Specialty Films Custom 205687-00N

P	S	S	2	0	5	6	8	7	-	0	0	N
MODEL			CUSTOM PART NUMBER							INTERNAL REVISION		VARIANT

A = AlN
B = BeO
F = ferrite/ garnet
K = zirconia
N = resistor conductor

Side Wall Patterning - Custom Substrate



CAPABILITIES

- Conductor patterning on 4 surfaces
- Wire-bondable or solderable metalizations
- Allows attachment to side wall of substrate
- Tight dimensional tolerances

APPLICATIONS

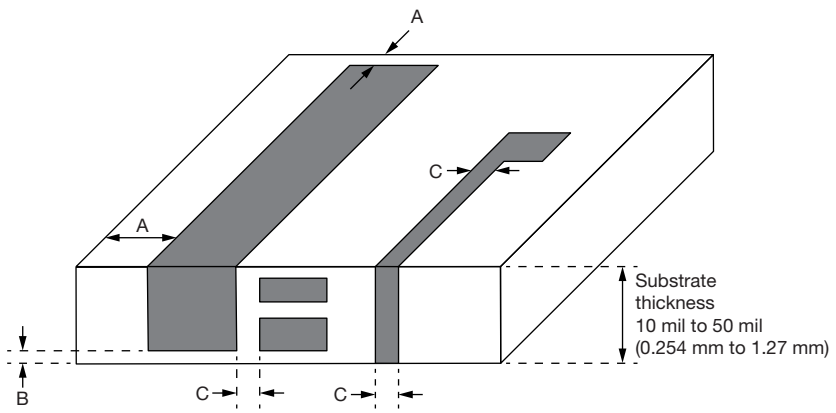
- Electro-mechanical or electro-optical applications that require an interface between the electric circuit and an element such as a mirror, lens, fiber, etc.
- High frequency circuits such as RF application, and high bit rate transceivers (TOSA / ROSA) that benefit by replacing wire bonds with side-patterned traces
- Applications that require a high degree of miniaturization

DESIGN SPECIFICATIONS AND RULES

- Substrate materials: alumina or AlN. Sidewall patterning can be deposited on plates ranging between 10 mils and 50 mils. Polished plates are preferred due to their tighter thickness tolerance.
- Metalization: TiW / Au, TiW / Ni / Au or TiW / Pd / Au as well as resistor and AuSn metalization available.
- Lines and gaps: lines and gaps down to 0.003" (75 microns) can be patterned on the component sidewalls.
- Pullback from bottom edge: traces designed to reach the bottom edge of the sidewall will requires a ± 2 mil tolerance. Positive tolerance represents a gap from the bottom edge; negative tolerance represents metal wrapping around edge to the rear surface.
- Geometric tolerances down to ± 1 mil (± 25 µm) can be maintained on sidewall geometries. Tolerances between metal on diced edges of the ceramic tile down to ± 2 mil.
- Connectivity: side wall patterns can be isolated (standalone), connected to front side only (half wrap) or connected to both front and rear sides (full wrap).
- Component with sidewall patterning can have integrated resistors or AuSn solder pads embedded on the front or rear surfaces. These capabilities are not allowed on the sidewall itself.

DESIGN SPECIFICATIONS	
Plate Thickness	0.010" to 0.050"
Minimum Gap	0.003"
Dimensional Tolerance	± 0.001"
Metal Pattern to Diced Edge Tolerance	≥ 0.002"
Metal Systems	TiW / Au / Au plate or TiW / Pd / Au
	TiW / Au / Ni plate / Au plate
	TaN / TiW / Au or NiCr / TiW / Au
	80 / 20 AuSn pads available, consult factory

SIDE WALL PATTERNING DESIGN RULES



A	B	C
Best alignment of metal to diced edges ± 0.002" (± 50 µm)	Metal pullback from bottom edge Typical: 0.002" ± 0.002" (50 µm ± 50 µm) or 0" ± 0.002" (0 µm ± 50 µm) Negative values wrap to rear side.	Line or gap 0.003" (75 µm) min. Typical tolerance: ± 0.002" (± 50 µm) Tight tolerance to ± 0.001" (± 25 µm) allowed in some cases

GLOBAL PART NUMBER INFORMATION

Global Part Numbering example: SDWP20xxxx-00Q

S	D	W	P	2	0					-	0	0	Q
Model				Sequential: assigned by factory						Internal revision			

Thin Film Metallized Plates - Custom Substrates

FEATURES

- Metalization on 1, 2, or 6 surfaces
- Various substrate materials
- Tantalum nitride or nickel chromium resistor material
- Sputtered / plated metal systems
- Sizes from 0.020" x 0.020" to 4.500" x 4.500"
- High volume
- Quick delivery available

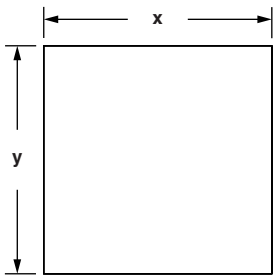
APPLICATIONS

Vishay EFI metalized plates can be used as stand-offs, jumpers or bonding pads in hybrid packages when diced to small sizes; they are also available with no metallization (bare ceramic) for use as spacers or insulators. Larger sized plates can be used where the customer wants to pattern and etch substrates in-house.

SUBSTRATE MATERIALS

MATERIAL CODE	MATERIAL	SURFACE FINISH (µ" CLA)		APPLICATION
A	Alumina (99.6)	A L P	< 3 front / < 4 back as-fired < 12 lapped < 1 polished	Cost effective material with wide range of applications
B	Beryllium oxide	L P	15 to 40 lapped < 3 polished	Highest thermal conductivity (285 W/mC)
N	Aluminum nitride	L P	10 to 20 lapped < 2 polished	High thermal conductivity (170 W/mC)

PLATE SIZE



X (mils)	Y (mils)
20	20
50	50
100	100
200	200
500	500
1000	1000
2000	2000
4500	4500

Note

- For any plates smaller than 1.000" x 1.000" or where plate size is not available, metal is only available on one or two surfaces (front or back)

RESISTOR MATERIAL

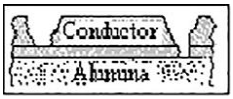
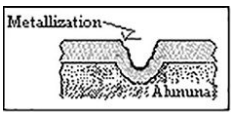
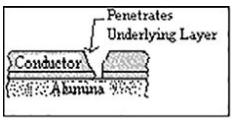
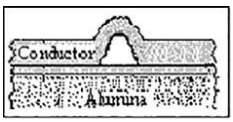
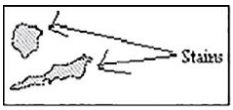
Typical reasons for using NiCr resistor material are for long term stability and high sheet rho. Typical recommended uses for TaN are for non-hermetic applications where self-passivation is important.

RESISTOR MATERIAL			
RESISTOR CODE	**RESISTOR MATERIAL**	**SHEET RHO (Ω/SQ) ± 20 %**	**TCR (ppm/°C) TYPICAL VALUES**
A	NiCr	25	± 50
B	NiCr	50	± 100
C	NiCr	100	± 200
D	NiCr	200	± 250
1	TaN	25	± 50
2	TaN	50	± 100
3	TaN	75	± 250

METAL STACK			
METAL CODE	**METAL STACK**	**TYPICAL APPLICATION**	**TYPICAL ATTACHMENT METHOD**
1	TiW (500 Å to 1000 Å) / Au (50 µ" min.)	Au and Al wirebondable	Epoxy
2	TiW (500 Å to 1000 Å) / Au (100 µ" min.)	Au and Al wirebondable	Epoxy
3	TiW (500 Å to 1000 Å) / Au (15 µ" to 40 µ") / Ni (20 µ" to 80 µ") / Au (50 µ" min.)	Au and Al wirebondable and solderable	Epoxy or solder
4	TiW (500 Å to 1000 Å) / Au (15 µ" to 40 µ") / Ni (20 µ" to 80 µ") / Au (100 µ" min.)	Au and Al wirebondable and solderable	Epoxy or solder
5	TiW (500 Å to 1000 Å) / Pd (1500 Å to 2500 Å) / Au (50 µ" min.)	Au and Al wirebondable and solderable	Epoxy or solder
6	TiW (500 Å to 1000 Å) / Pd (1500 Å to 2500 Å) / Au (100 µ" min.)	Au and Al wirebondable and solderable	Epoxy or solder
7	Cr (500 Å to 1500 Å) / Cu (5000 Å to 7000 Å) / Au (100 µ" min.)	Au and Al wirebondable	Epoxy
8	Cr (500 Å to 1500 Å) / Cu (500 u" min.) / Ni (20 µ" to 80 µ") / Au (100 µ" min.)	Au and Al wirebondable and solderable. High power applications for low metal resistivity	Epoxy or solder

VISUAL INSPECTION

VEFI uses internal visual inspection criteria as shown in the table below for metal non-patterned substrates. For any plates smaller than 1.000" x 1.000" or where plate size is not available, metal burrs will be acceptable along part edges where plates are sawn to size.

SURFACE PERFECTION INSPECTION CRITERIA (1)				
SCHEMATIC ILLUSTRATION	DEFECT TYPE	DEFECT SIZE	FRONT (2)	BACK (3)
	NODULES BUMPS	> 10 mil dia. (>0.254 mm)	0.25/sq"	0.25/sq"
		5 mil to 10 mil dia. (0.127 mm to 0.254 mm)	1/sq"	2/sq"
		3 mil to 5 mil dia. (0.076 mm to 0.127 mm)	3/sq"	6/sq"
		2 mil to 3 mil dia. (0.05 mm to 0.076 mm)	3/sq"	6/sq"
		< 2 mil dia. (< 0.05 mm)	NIF	NIF
	METALIZATION VOIDS PINHOLES	> 2 mil dia. (> 0.05 mm)	None	None
		1 mil to 2 mil dia. (0.0254 mm to 0.05 mm)	5/sq"	10/sq"
		< 1 mil high (< 0.0254 mm)	NIF	NIF
	CRATERS DEPRESSIONS (hole into ceramic)	> 10 mil dia. (> 0.254 mm)	None	None
		5 mil to 10 mil dia. (0.127 mm to 0.254 mm)	1/sq"	3/sq"
		2 mil to 5 mil dia. (0.05 mm to 0.127 mm)	4/sq"	4/sq"
		1 mil to 2 mil dia. (0.0254 mm to 0.05 mm)	15/sq"	15/sq"
		< 1 mil dia. (0.0254 mm)	NIF	NIF
	SCRATCHES (4) (excluding surface abrasions)	> 1/2 mil wide (> 0.0127 mm)	1/sq"	NIF
		< 1/2 mil wide (< 0.0127 mm)	NIF	NIF
	BLISTERS	> 10 mil dia. (> 0.254 mm)	None	None
		5 mil to 10 mil dia. (0.127 mm to 0.254 mm)	1/sq"	1/sq"
		2 mil to 5 mil dia. (0.05 mm to 0.127 mm)	2/sq"	2/sq"
		1 mil to 2 mil dia. (0.0254 mm to 0.05 mm)	4/sq"	4/sq"
		1/2 mil to 1 mil dia. (0.0127 mm to 0.0254 mm)	6/sq"	6/sq"
		1/4 mil to 1/2 mil dia. (0.006 mm to 0.0127 mm)	16/sq"	16/sq"
		< 1/4 mil dia. (< 0.006 mm)	NIF	NIF
	STAINS-SPOTS (5)	> 4 mil. (> 0.1 mm)	None	None
		2 mil to 4 mil (0.05 mm to 0.1 mm)	1/sq"	2/sq"
		1 mil to 2 mil (0.0254 mm to 0.05 mm)	2/sq"	4/sq"
		< 1 mil (< 0.0254 mm)	3/sq"	5/sq"

Notes

- NIF = not inspected for

(1) Exclusion area for 1" x 1" and greater plates: Front and Rear: 100 mils (2.54 mm) from substrate edge
(2) A-face 100 % inspection method: 3x to 8x magnification. Higher magnification may be used for defect verification
(3) B-face 100 % inspection method: Unaided eye. Higher magnification may be used for defect verification
(4) Scratch or probe mark exposing underlying material that is > 200 mils long
(5) Contamination: Not removable by distilled water or common solvents

GLOBAL PART NUMBER INFORMATION

Standard Global Part Number: SPF1AA02021A11BX

Global Part Number Description: SPF1 Al_2O_3 As-Fired 20 mils x 20 mils 10 mils Thick NiCr 25 Ω/sq Front: TiW / Au (50 µ" min.) Back: TiW / Au (50 µ" min.) BX

S	P	F	1	A	A	0	1	0	1	1	A	1	1	B	X

MODEL	MATERIAL	FINISH	PLATE SIZE X (MILS)	PLATE SIZE Y (MILS)	THICKNESS (MILS)	RESISTOR	METAL FRONT	METAL BACK	PACKAGING CODE
SPF1	**A** = Al_2O_3 **B** = BeO **N** = AlN	**A** = as-fired **L** = lapped **P** = polished	**02** = 20 **05** = 50 **10** = 100 **20** = 200 **50** = 500 **11** = 1000 **21** = 2000 **45** = 4500	**02** = 20 **05** = 50 **10** = 100 **20** = 200 **50** = 500 **11** = 1000 **21** = 2000 **45** = 4500	**1** = 10 **2** = 15 **3** = 20 **4** = 25	**N** = none Otherwise see Resistor Material table	**N** = none Otherwise see Metal Stack table	**N** = none Otherwise see Metal Stack table	**BX** = box 1 min. / 1 mult. **W1** = waffle pack 1 min. / 1 mult.

Custom Global Part Number: SPF1 xxxx - xx x

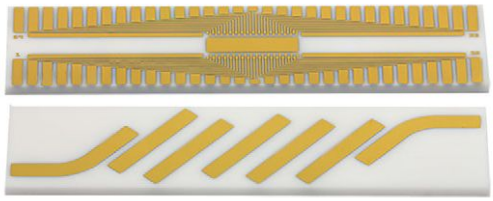
S	P	F	1						-			
MODEL				VEFI ASSIGNED NUMBER						INTERNAL REVISION		VARIANT

A = ALN
B = Be0
0 = coating

Note

- Plates 1" x 1" and greater will be individually packaged in glassine envelopes in the box

Custom Substrates - Conductor Pattern



FEATURES

- Precision conductor patterns
- Metalization on 1 or 2 surfaces
- Various substrate materials
- Sputtered / plated metal systems
- Custom sizes from 0.020" x 0.020" to 4.000" x 4.000"
- Quick delivery available

APPLICATIONS

Vishay EFI custom specialty films / conductor patterned substrates are used in the hybrid circuit and microwave industries. These conductor patterns are precisely manufactured to be used for complex fan-outs, interconnects, high temperature, and RF / microwave designs. Vishay EFI custom specialty films / conductor patterned substrates can also be used in a wider variety of applications including jumpers, mounting pads, and bonding pads. The custom specialty film / conductor patterned substrates are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The custom specialty film / conductor patterned substrates are visually inspected to MIL-STD-883, method 2032 class H or K.

DEFINING A METAL SYSTEM

Vishay EFI offers several different metals to meet the custom needs of our customers. Simple conductor circuits have the most flexibility with available metal systems. As the complexity and level of integration increase, the list of available metal system choices is limited to allow for tighter process control and manufacturability. The following table identifies the specific function of the available metals as well as their available thickness ranges.

AVAILABLE METALS AND THEIR FUNCTIONS

LAYER TYPE	METAL	RANGE OF VALUES	COMMENTS
Adhesion	Titanium tungsten (TiW)	500 Å to 1250 Å	Ideal for high temperatures
	Chromium (Cr)	500 Å to 1250 Å	Ideal for low temperatures
Barrier	Nickel (Ni)	1250 Å to 1750 Å	Sputtered barrier
	Palladium (Pd)	1500 Å to 2500 Å	High temperature solder barrier
Conductor	Gold (Au)	10 µ" to 200 µ" (0.25 µm to 5 µm)	-
	Copper (Cu)	20 µ" to 200 µ" (0.05 µm to 5 µm)	-
	Aluminum (Al)	50 µ" to 120 µ" (1.27 µm to 5 µm)	Aluminum wire bond
High Current Conductor	Gold (Au)	200 µ" to 1000 µ" (5 µm to 25 µm)	Gold wire bond
	Copper (Cu)	200 µ" to 4000 µ" (5 µm to 100 µm)	High temperature / conductivity

Note

- TaN and NiCr are available as adhesion metal layers under certain metal stacks. Call factory for details

APPLICATION OF METAL SYSTEMS

A metal system should be selected based upon electrical, thermal, and mechanical performance demands as well as the assembly process requirements. Assembly requirements might include pads suitable for eutectic (solder) bonding and / or wire bonding.

Soldering pads should include a barrier layer designed to control the solubility of the pad metallization with the solder being applied. A nickel or palladium barrier layer is typically deposited under gold soldering pads to ensure reliable device attachment due to gold's high solubility in solders.

All of the standard metal systems offered by Vishay EFI are readily bonded using gold wire. For optimal bond integrity, a minimum of 100 µ" (2.5 µm) gold thickness is recommended, although reasonable bonding results can be achieved with gold as thin as 50 µ" (1.2 µm).

Intermetallic formation and barrier metal migration are influenced by film exposure to high temperatures. For this reason, it is important to select a metal system that can withstand the temperature profile requirements of the application. The following table provides a matrix of standard metal systems and assembly options.

STANDARD METAL SYSTEMS AND ASSEMBLY OPTIONS

METAL SYSTEM	MAX. REFLOW TEMPERATURE	WIRE-BONDABLE GOLD	SOLDER TYPE	
			LEAD / LEAD (Pb)-FREE	GOLD BEARING
Cr / Cu / Ni / Au	350	Yes	Preferred	Yes
NiCr / TiW / Au	400	Yes	-	Yes
NiCr / Ni / Au	350	Yes	Preferred	Yes
NiCr / TiW / Au / Ni / Au	350	Yes	Preferred	Yes
TiW / Au	450	Yes	-	Yes
TiW / Ni / Au	350	Yes	Preferred	Yes
TiW / Au / Ni / Au	350	Yes	Preferred	Yes
TiW / Pd / Au	450	Yes	Yes	Preferred
TiW / Au / Cu / Ni / Au	350	Yes	Preferred	Yes
TaN / TiW / Au	450	Yes	-	Yes
TaN / TiW / Ni / Au	350	Yes	Preferred	Yes
TaN / TiW / Au / Ni / Au	350	Yes	Preferred	Yes
TaN / TiW / Pd / Au	450	Yes	Yes	Preferred
TaN / TiW / Au / Cu / Ni / Au	350	Yes	Preferred	Yes

Additional metal system capabilities are available. These options are subject to review by the Vishay EFI engineering and production teams. Consideration will be given to special requests, with a focus on manufacturability and reliability.

INCORPORATING HIGH CONDUCTIVITY TRACES

Vishay EFI's capability to deposit thick conductor traces has enabled design approaches that allow high current, low resistance circuit traces to co-exist with microwave structures and transmission lines. For circuit traces carrying high currents over long distances, the resistive losses of thin film conductor lines can become significant. By selectively increasing the thickness of high-current lines, the engineer can have fine line RF structures on the same circuit with low-loss DC lines. Additionally, these low-resistance traces can be used to manage thermal loads within RF circuits.

Typically, the design engineer will calculate the trace resistance (R_{total}) of a structure during the design process. The trace resistance is defined as:

R_{total} = (trace length / trace width) x conductor sheet resistance
R_{total} = (L / W) x R_{sheet}.

The sheet resistance (R_{sheet}) is derived by dividing the bulk resistivity by the conductor thickness. Therefore, the thicker one can deposit the conductor, the lower the overall sheet resistance. The following two tables detail the bulk resistivity and the typical sheet resistance of some common thin film metals at a variety of deposition thicknesses.

SELECTED BULK RESISTIVITY		
MATERIAL	**THEORETICAL BULK RESISTIVITY μΩ x cm**	**CONSERVATIVE VALUE OF BULK RESISTIVITY WHEN DEPOSITED μΩ x cm**
Gold (Au)	2.2	2.4 (sputtered) / 2.9 (plated)
Titanium Tungsten (TiW)	-	45 (sputtered)
Copper (Cu)	1.71	2 (sputtered) / 4 (plated)
Nickel (Ni)	7	8.2 (sputtered)
Aluminum (Al)	2.7	3 (sputtered)

SELECTED APPROXIMATE SHEET RESISTIVITIES		
METAL	**THICKNESS μ" (μm)**	**PLATED SHEET RESISTIVITY (mΩ /sq)**
Gold (Au)	80 (2)	14.5
Gold (Au)	160 (4)	7.25
Gold (Au)	400 (10)	2.9
Copper (Cu)	1000 (25)	0.42
Copper (Cu)	2000 (50)	0.21
Nickel (Ni)	200 (5)	160 (sputtered)
Aluminum (Al)	40 (1)	30 (sputtered)

In summary, gold (Au) and copper (Cu) can be deposited at much greater thicknesses than standard thin films to reduce overall conductor resistance. Gold (Au) can be deposited up to a maximum thickness of 400 μ", while copper (Cu) can be plated routinely at thicknesses up to 4000 μ" (100 μm). It is important to note that minimum line widths and spaces increase with film thickness. See the following for a summary of line widths and spaces as associated with conductor thickness.

PATTERNING LINES AND SPACES

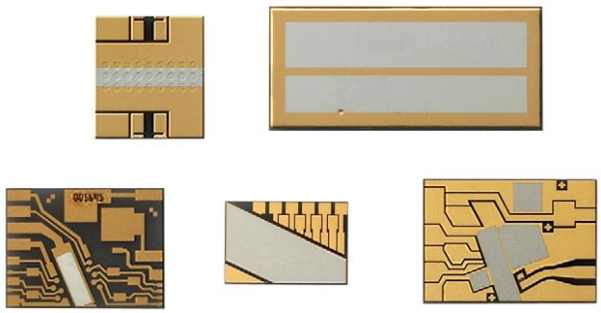
Thin film patterning tolerances are influenced by several factors in the photomasking process. Pattern tolerancing for plating and etching processes vary based on the metal thickness as shown in the tables below. As the thickness of the metal increases, the photoresist used for this process changes and the metal thickness tolerances and line and space patterning must be adjusted to compensate for this. As these decisions are made the surface finish of the substrate must also be factored as the polished surface finish will deliver the smoothest surface and therefore the best line and space pattern. For the substrate materials where As fired and lapped options are available these surfaces will not hold the same tolerances and minimum sizes that the polished surface will.

PLATED METAL PATTERNS			
TOTAL MAX. METAL THICKNESS	**BEST PATTERN TOLERANCE PROCESS**	**BEST PLATING THICKNESS TOLERANCE**	**SMALLEST PATTERN LINE AND SPACE**
100 μ" (2.54 μm)	± 0.1 mil	± 30 μ"	0.5 mil / 0.5 mil
150 μ" (3.8 μm)	± 0.15 mil	± 40 μ"	0.5 mil / 0.5 mil
250 μ" (6.35 μm)	± 0.2 mil	± 50 μ"	0.5 mil / 0.5 mil
400 μ" (10.2 μm)	± 0.2 mil	± 100 μ"	0.5 mil / 0.5 mil
800 μ" (20.3 μm)	0.3 mil±	± 150 μ"	1 mil / 1 mil
1000 μ" (25.4 μm)	± 1.0 mil	± 250 μ"	2 mil / 2 mil
2000 μ" (51 μm)	± 2.0 mil	± 500 μ"	3 mil / 3 mil
4000 μ" (102 μm)	± 3.0 mil	± 1 mil	5 mil / 5 mil

ETCHED METAL PATTERNS				
TOTAL MAX. METAL THICKNESS	BEST PATTERN TOLERANCE PROCESS	BEST METAL THICKNESS TOLERANCE	SMALLEST PATTERN LINE AND SPACE	METAL DEPOSITION
100 µ" (2.54 µm)	± 0.1 mil	Ref. plating table	1 mil / 1 mil	Plated
150 µ" (3.8 µm)	± 0.2 mil	Ref. plating table	1.5 mil / 1.5 mil	Plated
200 µ" (5.1 µm)	± 0.3 mil	Ref. plating table	2 mil / 2 mil	Plated
300 µ" (7.6 µm)	± 0.5 mil	Ref. plating table	2 mil / 2 mil	Plated
12 000 Å	± 0.5 mil	±10 %	1.5 mil / 2 mil	Sputtered
25 000 Å	± 1.0 mil	±10 %	2 mil / 2 mil	Sputtered

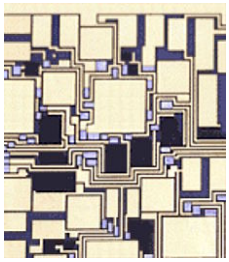
AuSn APPLICATIONS

Vishay EFI offers the option of a sputter deposition of gold-tin solder with wt % of 80 / 20 while maintaining tolerances tighter than ± 2 % wt and control of film thickness to ± 1.0 µm. This capability allows deposition of customer AuSn patterns that can be used to fine-tune assembly processes to meet the most demanding requirements; the tight composition tolerance eliminates the need to adjust reflow process parameters to compensate for variations in solder composition. The gold-tin deposition process allows films with thickness ranging between 4.5 µm and 7 µm with a tolerance of ± 1.0 µm. Common applications for AuSn deposition are laser diode sub-mounts, fiber optic pump lasers, optical transmitters, optical receivers, optical transceivers and optical TOSA / ROSA packages.



HIGH TEMPERATURE APPLICATIONS

When designing hybrid assemblies to operate at temperatures above 125 °C it becomes important to provide monometallic interconnects to prevent intermetallic diffusion and resultant long term reliability problems. For these situations, Vishay Electro-Films (EFI) has developed processes for depositing both aluminum and gold bonding pads on the same substrate. This structure provides for monometallic interconnects. Aluminum wire can be used to connect from the aluminum pads on the substrate. Similarly, gold wire can be used to connect gold pads on the substrate to gold hermetic package terminals. Appropriate barrier metals are included in substrate processing to provide long term reliability in high temperature applications.



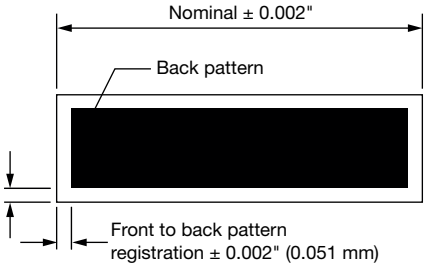
High temperature - Au and Al wirebond pads

SUBSTRATE SINGULATION

Vishay Electro-Films uses standard semiconductor / ceramic dicing equipment and processes to singulate production boards into individual pieces. These processes depend on tight alignment and inspection to maintain overall part dimension tolerances and metal pattern to part edge tolerances. Each of these dimensions and their tolerances are measured on each lot that is processed.

SUBSTRATE SINGULATION

DIMENSION	DIMENSION MEASUREMENT in inches (mm)	MINIMUM TOLERANCE in inches (mm)
Metal pattern pullback from edge of die	0.002 (0.0508)	± 0.002 (± 0.0508)
Overall part dimension	n/a	± 0.002 (± 0.0508)
Front to back pattern tolerance	n/a	± 0.002 (± 0.0508)



GLOBAL PART NUMBER INFORMATION

Custom Global Part Number: SPF2 05687 - 00 C

Custom Global Part Number Description: Specialty Films Custom 205687-00C

S	P	F	2	0	5	6	8	7	-	0	0	C

- MODEL (S P F 2)
- CUSTOM PART NUMBER (0 5 6 8 7)
- INTERNAL REVISION (0 0)
- VARIANT (C)
  - **A** = AlN
  - **B** = BeO
  - **C** = conductor
  - **F** = ferrite/ garnet
  - **K** = zirconia

По вопросам продаж и поддержки обращайтесь:

Алматы (7273)495-231
Архангельск (8182)63-90-72
Астрахань (8512)99-46-04
Барнаул (3852)73-04-60
Белгород (4722)40-23-64
Брянск (4832)59-03-52
Владивосток (423)249-28-31
Волгоград (844)278-03-48
Вологда (8172)26-41-59
Воронеж (473)204-51-73
Екатеринбург (343)384-55-89
Иваново (4932)77-34-06
Ижевск (3412)26-03-58
Иркутск (395)279-98-46
Казань (843)206-01-48
Калининград (4012)72-03-81
Калуга (4842)92-23-67
Кемерово (3842)65-04-62
Киров (8332)68-02-04
Краснодар (861)203-40-90
Красноярск (391)204-63-61
Курск (4712)77-13-04
Липецк (4742)52-20-81
Магнитогорск (3519)55-03-13
Москва (495)268-04-70
Мурманск (8152)59-64-93
Набережные Челны (8552)20-53-41
Нижний Новгород (831)429-08-12
Новокузнецк (3843)20-46-81
Новосибирск (383)227-86-73
Омск (3812)21-46-40
Орел (4862)44-53-42
Оренбург (3532)37-68-04
Пенза (8412)22-31-16
Пермь (342)205-81-47
Ростов-на-Дону (863)308-18-15
Рязань (4912)46-61-64
Самара (846)206-03-16
Санкт-Петербург (812)309-46-40
Саратов (845)249-38-78
Севастополь (8692)22-31-93
Симферополь (3652)67-13-56
Смоленск (4812)29-41-54
Сочи (862)225-72-31
Ставрополь (8652)20-65-13
Сургут (3462)77-98-35
Тверь (4822)63-31-35
Томск (3822)98-41-53
Тула (4872)74-02-29
Тюмень (3452)66-21-18
Ульяновск (8422)24-23-59
Уфа (347)229-48-12
Хабаровск (4212)92-98-04
Челябинск (351)202-03-61
Череповец (8202)49-02-64
Ярославль (4852)69-52-93

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